WHAT IS CLAIMED IS:

1. A demodulating circuit for demodulating a pulse signal including runs of identical '1' or '0' symbols, comprising:

a differentiating circuit for detecting voltage changes at rising and falling transitions of the pulse signal and outputting a differentiated signal responsive to the voltage changes; and

a hysteresis comparator for comparing the differentiated signal with a first reference voltage according to a predetermined upper threshold voltage higher than the first reference voltage and a predetermined lower threshold voltage lower than the first reference voltage, thereby generating a demodulated signal that maintains a first logic level when the differentiated signal is above the upper threshold voltage, maintains a second logic level when the differentiated signal is below the lower threshold level, and maintains an existing one of the first and second logic levels without changing when the differentiated voltage is between the upper threshold voltage and the lower threshold voltage.

2. The demodulating circuit of claim 1, wherein:

the hysteresis comparator comprises

a comparator element having an inverting input terminal for receiving the first reference voltage, a non-inverting input terminal for receiving the differentiated signal, and an output terminal for output of the demodulated signal,

a first resistance element coupling the output terminal of the comparator element to the non-inverting input terminal of the comparator element, and

a second resistance element coupling the first reference voltage to the non-inverting input terminal of the comparator element;

and the differentiating circuit comprises

a differentiating capacitor coupling the pulse signal to the non-inverting input terminal of the comparator element, and

a compound resistance for charging and discharging the differentiating capacitor, the compound resistance including the first resistance element and the second resistance element.

3. The demodulating circuit of claim 1, wherein:

the hysteresis comparator comprises

a comparator element having an inverting input terminal for receiving the differentiated signal, a non-inverting input terminal for receiving the first reference voltage used for voltage comparison, and an output terminal for output of the demodulated signal;

a first resistance element coupling the output terminal of the comparator element to the non-inverting input terminal of the comparator element, and

a second resistance element coupling the first reference voltage to the non-inverting input terminal of the comparator element;

and the differentiating circuit comprises

a differentiating capacitor coupling the pulse signal to the inverting input terminal of the comparator element, and

a third resistance element coupling the first reference voltage to the inverting input terminal of the comparator element, for charging and discharging the differentiating capacitor.

4. The demodulating circuit of claim 1, wherein:

the hysteresis comparator comprises

a comparator element having an inverting input terminal

for receiving the differentiated signal, a non-inverting input terminal for receiving the first reference voltage, and an output terminal for output of the demodulated signal,

a first resistance element coupling the output terminal of the comparator element to the non-inverting input terminal of the comparator element, and

a second resistance element coupling the first reference voltage to the non-inverting input terminal of the comparator element;

and the differentiating circuit comprises

an inverting amplifier having an input terminal and an output terminal, the differentiated signal being output from the output terminal of the inverting amplifier,

a negative feedback resistance element coupled between the input and output terminals of the inverting amplifier, and

a differentiating capacitor coupling the pulse signal to the input terminal of the inverting amplifier.

5. The demodulating circuit of claim 1, wherein:

the differentiating circuit outputs the differentiated signal as a positive-phase differentiated signal;

the differentiating circuit also outputs a negative-phase differentiated signal complementary to the positive-phase differentiated signal;

the hysteresis comparator includes a balanced comparator element having a non-inverting input terminal for receiving the positive-phase differentiated signal and an inverting input terminal for receiving the negative-phase differentiated signal;

the balanced comparator element outputs the demodulated signal as a positive-phase demodulated signal; and

the balanced comparator element also outputs a negative-phase demodulated signal complementary to the

positive-phase demodulated signal.

6. The demodulating circuit of claim 5, wherein:

the hysteresis comparator further comprises

first and second resistance elements for dividing a potential difference between the positive-phase demodulated signal and the first reference voltage to provide positive feedback at the non-inverting input terminal of the balanced comparator element, and

third and fourth resistance elements for dividing a potential difference between the negative-phase demodulated signal and the first reference voltage to provide positive feedback at the inverting input terminal of the balanced comparator element;

and the differentiating circuit comprises

a differentiating capacitor coupling the pulse signal to the non-inverting input terminal of the balanced comparator element, and

a compound resistance, including the first, second, third, and fourth resistance elements, for charging and discharging the differentiating capacitor.

7. The demodulating circuit of claim 5, wherein:

the differentiating circuit comprises

a differential amplifier having a non-inverting input terminal and an inverting input terminal, for generating the positive-phase differentiated signal and the negative-phase differentiated signal in response to a potential difference between the non-inverting input terminal and the inverting input terminal,

a first negative feedback resistance element coupling the negative-phase differentiated signal to the non-inverting input terminal of the differential amplifier,

a second negative feedback resistance element coupling

the positive-phase differentiated signal to the inverting input terminal of the differential amplifier,

a first differentiating capacitor coupling the pulse signal to the non-inverting input terminal of the differential amplifier, and

a second differentiating capacitor coupling a ground potential to the inverting input terminal of the differential amplifier;

and the hysteresis comparator further comprises

first and second resistance elements for dividing a potential difference between the positive-phase demodulated signal output and the positive-phase differentiated signal to provide positive feedback at the non-inverting input terminal of the balanced comparator element, and

third and fourth resistance elements for dividing a potential difference between the negative-phase demodulated signal and the negative-phase differentiated signal to provide positive feedback at the inverting input terminal of the balanced comparator element;

the positive-phase demodulated signal assuming the first logic level when either the positive-phase differentiated signal goes above the upper threshold level or the negative-phase differentiated signal goes below the lower threshold voltage;

the positive-phase demodulated signal assuming the second logic level when either the positive-phase differentiated signal goes below the lower threshold level or the negative-phase differentiated signal goes above the upper threshold voltage.

8. The demodulating circuit of claim 5, wherein the differentiating circuit comprises a differential signal generating circuit having a non-inverting input terminal for receiving the pulse signal and an inverting input terminal

for receiving a second reference voltage, the differential signal generating circuit generating a positive-phase differential signal and a negative-phase differential signal responsive to a potential difference between the pulse signal and the second reference voltage, the positive-phase differentiated signal being generated from the positive-phase differential signal, the negative-phase differentiated signal being generated from the negative-phase differential signal.

9. The demodulating circuit of claim 8, wherein:

the hysteresis comparator further comprises

first and second resistance elements for dividing a potential difference between the positive-phase demodulated signal and the first reference voltage to provide positive feedback at the non-inverting input terminal of the balanced comparator element, and

third and fourth resistance elements for dividing a potential difference between the negative-phase demodulated signal and the first reference voltage to provide positive feedback at the inverting input terminal of the balanced comparator element;

and the differentiating circuit further comprises

a first differentiating capacitor coupling the positive-phase differential signal to the non-inverting input terminal of the balanced comparator element, and

a second differentiating capacitor coupling the negative-phase differential signal to the inverting input terminal of the balanced comparator element.

10. The demodulating circuit of claim 8, wherein:

the differentiating circuit further comprises

a differential amplifier having a non-inverting input terminal and an inverting input terminal, for generating the

positive-phase differentiated signal and the negative-phase differentiated signal in response to a potential difference between the non-inverting input terminal and the inverting input terminal,

a first negative feedback resistance element coupling the negative-phase differentiated signal to the non-inverting input terminal of the differential amplifier,

a second negative feedback resistance element coupling the positive-phase differentiated signal to the inverting input terminal of the differential amplifier,

a first differentiating capacitor coupling the positive-phase differential signal to the non-inverting input terminal of the differential amplifier, and

a second differentiating capacitor coupling the negative-phase differential signal to the inverting input terminal of the differential amplifier;

and the hysteresis comparator further comprises

first and second resistance elements for dividing a potential difference between the positive-phase demodulated signal and the positive-phase differentiated signal to provide positive feedback at the non-inverting input terminal of the balanced comparator element, and

third and fourth resistance elements for dividing a potential difference between the negative-phase demodulated signal and the negative-phase differentiated signal to provide positive feedback at the inverting input terminal of the balanced comparator element.

11. The demodulating circuit of claim 1, wherein the differentiating circuit comprises:

an inverting amplifier having an input terminal and an output terminal;

a negative feedback resistance element coupled between the input and output terminals of the inverting amplifier;

a differentiating capacitor connected to the input terminal of the inverting amplifier; and

a resistance element connected in series with the differentiating capacitor, for adjusting a differentiating characteristic of the differentiating circuit.

12. The demodulating circuit of claim 1, wherein the differentiating circuit comprises a limiting element for limiting an amplitude of the differentiated signal.

13. The demodulating circuit of claim 1, wherein the hysteresis comparator comprises:

a positive feedback element providing positive feedback of the demodulated signal; and

a limiting element for limiting an amplitude of the positive feedback.

14. The demodulating circuit of claim 1, wherein the differentiating circuit includes a low-pass filter for removing high-frequency noise from the pulse signal.

15. The demodulating circuit of claim 1, wherein the hysteresis comparator comprises:

a logic state holding unit operating with hysteresis to generate an intermediate signal having a first state and a second state; and

a logic level converting unit for converting the first state of the intermediate signal to the first logic level and converting the second state of the intermediate signal to the second logic level, thereby generating the demodulated signal.

16. The demodulating circuit of claim 15, wherein the logic state holding unit comprises:

an input circuit for receiving the differentiated signal and switching the intermediate signal between the first state and the second state; and

a positive feedback circuit for holding the intermediate signal in the state to which the intermediate signal is switched by the input circuit.

17. An optical receiving circuit using the demodulating circuit of claim 1 to receive a burst optical signal used in optical communication.